1. A chip carrier comprising:

an interposer element comprising a semiconductor substrate layer and at least one insulating layer on a surface of said substrate layer, said insulating layer supporting at least one passive circuit element which is separated from said substrate layer by a portion of said insulating layer, said portion of said insulating layer having a thickness which is sufficient to electrically shield said at least one passive circuit element from said substrate layer.

2. The chip carrier of claim 1, further comprising at least one integrated circuit chip attached to said interposer element and electrically connected to said at least one passive circuit element.

3. The chip carrier of claim 2, wherein said semiconductor substrate layer comprises a silicon layer.

4. The chip carrier of claim 3, wherein said at least one insulating layer comprises an oxide layer.

5. The chip carrier of claim 4, wherein said oxide layer includes silicon dioxide (SiO_2).

6. The chip carrier of claim 5, wherein said oxide layer has a thickness within a range of three to five microns.

7. The chip carrier of claim 3, wherein said at least one insulating layer comprises a polyamide layer.

8. The chip carrier of claim 3, wherein said at least one passive element is embedded within said at least one insulating layer.

9. The chip carrier of claim 3, wherein said at least one passive element is formed on said at least one insulating layer.

10. The chip carrier of claim 3, further comprising a metallization pattern on or within said insulating layer connected with said at least one passive circuit device.

11. The chip carrier of claim 3, wherein said at least one insulating layer includes a plurality of passive circuit elements, said plurality of passive circuit elements separated from said substrate layer by a portion of said at least one insulating layer, said portion of said at least one insulating layer having a thickness such that said plurality of passive circuit elements are electrically shielded from the conductance of said substrate layer.

12. The chip carrier of claim 11, wherein said plurality of passive circuit elements includes a resistor element.

13. The chip carrier of claim 12, wherein said resistor element is a thin film metal resistor.

14. The chip carrier of claim 13, wherein said plurality of passive circuit elements includes a capacitor element.

15. The chip carrier of claim 14, wherein said capacitor element is a thin film capacitor.

16. The chip carrier of claim 15, wherein said thin film capacitor includes a dielectric layer.

17. The chip carrier of claim 16, wherein said dielectric layer is an oxide composition.

18. The chip carrier of claim 16, wherein said dielectric layer is an oxide-nitride-oxide composition.

19. The chip carrier of claim 15, wherein said plurality of passive circuit elements includes an inductor element.

20. The chip carrier of claim 19, wherein said inductor element is a spiral inductor.

21. The chip carrier of claim 20, wherein said plurality of passive circuit elements form at least one passive circuit device, said passive circuit device having at least one of said plurality of passive circuit elements and electrically connected to said at least one integrated circuit chip.

22. The chip carrier of claim 21, wherein said plurality of passive circuit elements form at least one passive circuit device used in radio frequency (RF) communications systems.

23. The chip carrier of claim 22, wherein said interposer element and said at least one integrated circuit are arranged to form circuitry used in RF communications systems.

24. The chip carrier of claim 23, wherein said at least one passive circuit device comprises a load amplifier.

25. The chip carrier of claim 23, wherein said at least one passive circuit device comprises a broad band amplifier.

26. The chip carrier of claim 23, wherein said at least one passive circuit device comprises an oscillator.

27. The chip carrier of claim 26, wherein said oscillator is a voltage controlled oscillator.

28. The chip carrier of claim 23, wherein said at least one integrated circuit chip comprises a chip having at least one logic device electrically connected to said interposer element.

29. The chip carrier of claim 28, wherein said chip contains analog circuitry.

30. The chip carrier of claim 28, wherein said at least one logic device is a transistor.

31. The chip carrier of claim 30, wherein said chip contains digital circuitry.

32. The chip carrier of claim 31, wherein said chip is a microprocessor.

33. The chip carrier of claim 31, wherein said chip is a memory chip.

34. The chip carrier of claim 29, wherein said at least one integrated circuit chip is attached to said interposer element by solder joints.

35. The chip carrier of claim 34, wherein said at least one integrated circuit chip is attached to said interposer element through flip-chip bonding.

36. The chip carrier of claim 35, wherein said solder joints have varying compositions such that each of said solder joints has a selective melting temperature.

37. The chip carrier of claim 29, wherein said at least one integrated circuit chip is attached to said interposer element by a conductive adhesive substance.

38. The chip carrier of claim 29, wherein a bonding agent is located in the area between the said at least one integrated circuit chip and said insulating layer.

39. The chip carrier of claim 38, wherein said bonding agent is epoxy.

40. The chip carrier of claim 29, wherein said chip carrier is encapsulated to form a circuit package, said circuit package having conducting leads on an outer side of said package.

41. The chip carrier of claim 40, further comprising conductive leads connecting the chip carrier to said conductive package leads of said circuit package.

42. The chip carrier of claim 2, wherein said interposer element includes first and second insulating layers on opposing surfaces of said substrate.

43. The chip carrier of claim 42, wherein each of said first and second insulating layers has at least one passive circuit element separated from said substrate layer by a portion of said first and second insulating layers having a thickness such that each of said at least one passive circuit elements is electrically shielded from the conductance of said substrate layer.

44. The chip carrier of claim 43 wherein said first and second insulating layers include a plurality of passive circuit elements.

45. The chip carrier of claim 44, wherein at least one of said first and second insulating layers has at least one active circuit element.

46. The chip carrier of claim 1, wherein said substrate layer is comprised of gallium-arsenide.

47. The chip carrier of claim 46, wherein said insulating layer is comprised of gallium-arsenide-oxide.

48. A chip carrier comprising:

an interposer element comprising a semiconductor substrate layer and at least one insulating layer on a surface of said substrate layer, said insulating layer supporting at least one passive circuit element which is separated from said substrate layer by a portion of said insulating layer, said portion of said insulating layer having a thickness which is sufficient to electrically shield said at least one passive circuit element from said substrate layer;

at least one integrated circuit chip attached to said interposer element and electrically connected to said at least one passive circuit element; and

said interposer element and said at least one integrated circuit contain electrical elements which form circuitry for use in radio frequency (RF) communications systems.

49. The chip carrier of claim 48, wherein at least one of said plurality of insulating layers comprises an oxide layer.

50. The chip carrier of claim 49, wherein said oxide layer includes silicon dioxide (SiO_2).

51. The chip carrier of claim 50, wherein said oxide layer has a thickness within a range of three to five microns.

52. The chip carrier of claim 48, wherein at least one of said plurality of insulating layers comprises a polyamide layer.

53. The chip carrier of claim 48, wherein at least one of said plurality of passive elements is embedded within said at least one insulating layer.

54. The chip carrier of claim 48, wherein at least one of said plurality of passive elements is formed on said at least one insulating layer.

55. The chip carrier of claim 48, further comprising a metallization pattern on or within said insulating layer connected with said at least one passive circuit device.

56. The chip carrier of claim 55, wherein said plurality of passive circuit elements includes a resistor element.

57. The chip carrier of claim 56, wherein said resistor element is a thin film metal resistor.

58. The chip carrier of claim 57, wherein said plurality of passive circuit elements includes a capacitor element.

59. The chip carrier of claim 58, wherein said capacitor element is a thin film capacitor.

60. The chip carrier of claim 59, wherein said thin film capacitor includes a dielectric layer.

61. The chip carrier of claim 60, wherein said dielectric layer is an oxide composition.

62. The chip carrier of claim 60, wherein said dielectric layer is an oxide-nitride-oxide composition.

63. The chip carrier of claim 60, wherein said plurality of passive circuit elements includes an inductor element.

64. The chip carrier of claim 63, wherein said inductor element is a spiral inductor.

65. The chip carrier of claim 64, wherein said plurality of passive circuit elements form at least one passive circuit device, said passive circuit device having at least one of said plurality of passive circuit elements and electrically connected to said at least one integrated circuit chip.

66. The chip carrier of claim 65, wherein said plurality of passive circuit elements form at least one passive circuit device used in radio frequency (RF) communications systems.

67. The chip carrier of claim 66, wherein said at least one passive circuit device comprises a load amplifier.

68. The chip carrier of claim 66, wherein said at least one passive circuit device comprises a broad band amplifier.

69. The chip carrier of claim 66, wherein said at least one passive circuit device comprises an oscillator.

70. The chip carrier of claim 69, wherein said oscillator is a voltage controlled oscillator.

71. The chip carrier of claim 66, wherein said at least one integrated circuit chip comprises a chip having at least one logic device electrically connected to said interposer element.

72. The chip carrier of claim 71, wherein said chip contains analog circuitry.

73. The chip carrier of claim 71, wherein said at least one logic device is a transistor.

74. The chip carrier of claim 73, wherein said chip contains digital circuitry.

75. The chip carrier of claim 74, wherein said chip is a microprocessor.

76. The chip carrier of claim 74, wherein said chip is a memory chip.

77. The chip carrier of claim 71, wherein said at least one integrated circuit chip is attached to said interposer element by solder joints.

78. The chip carrier of claim 77, wherein said at least one integrated circuit chip is attached to said interposer element through flip-chip bonding.

79. The chip carrier of claim 78, wherein said solder joints have varying compositions such that each of said solder joints has a selective melting temperature.

80. The chip carrier of claim 71, wherein said at least one integrated circuit chip is attached to said interposer element by a conductive adhesive substance.

81. The chip carrier of claim 71, wherein a bonding agent is located in the area between the said at least one integrated circuit chip and said insulating layer.

82. The chip carrier of claim 81, wherein said bonding agent is epoxy.

83. The chip carrier of claim 71, wherein said chip carrier is encapsulated to form a circuit package, said circuit package having conducting leads on an outer side of said package.

84. The chip carrier of claim 83, further comprising conductive leads connecting the chip carrier to said conductive package leads of said circuit package.

85. The chip carrier of claim 71, wherein said interposer element includes first and second insulating layers on opposing surfaces of said silicon substrate.

86. The chip carrier of claim 85, wherein each of said first and second insulating layers has a plurality of passive circuit elements separated from said silicon substrate layer by a portion of said first and second insulating layers having a thickness such that said plurality of passive circuit elements are electrically shielded from the conductance of said silicon substrate layer.

87. The chip carrier of claim 86, wherein at least one of said first and second insulating layers has at least one active circuit element.

88. A process for forming an interposer element for use as a chip carrier comprising the steps of:

providing an insulating layer on at least one surface of a silicon substrate; and

processing said insulating layer to produce at least one passive circuit element on or within said insulating layer, said at least one passive circuit element being separated from said silicon substrate by a portion of said insulating layer, said portion of said insulating layer having a thickness such that said at least one passive circuit element is electrically shielded from said silicon substrate.

89. The process according to claim 88, further comprising the step of bonding at least one integrated circuit chip to the interposer element such that said at least one integrated circuit chip is electrically connected to said at least one passive circuit element.

90. The process according to claim 89, wherein said step of bonding comprises solder bonding.

91. The process according to claim 90, wherein said step of bonding comprises flip-chip bonding.

92. The process according to claim 89, wherein said insulating layer is formed of an oxide.

93. The process according to claim 92, wherein said oxide is silicon dioxide (SiO_2).

94. The process according to claim 93, wherein said insulating layer has a thickness within a range of three to five microns.

95. The process according to claim 89, wherein said insulating layer is formed of polyamide.

96. The process according to claim 89, further comprising the step of forming a metallization pattern on or within said insulating layer, said metallization pattern connected with said at least one passive circuit element.

97. The process according to claim 96, wherein said step of processing said insulating layer further comprises the step of producing a plurality of passive circuit elements on or within said insulating layer.

98. The process according to claim 97, wherein said plurality of passive circuit elements includes a resistor element.

99. The process according to claim 98, wherein said resistor element is a thin film metal resistor.

100. The process according to claim 97, wherein said plurality of passive circuit elements includes a capacitor element.

101. The process according to claim 100, wherein said capacitor element is a thin film capacitor.

102. The process according to claim 101, wherein said thin film capacitor includes a dielectric layer.

103. The process according to claim 102, wherein said dielectric layer is an oxide composition.

104. The process according to claim 102, wherein said dielectric layer is an oxide-nitride-oxide composition.

105. The process according to claim 97, wherein said plurality of passive circuit elements includes an inductor element.

106. The process according to claim 105, wherein said inductor element is a spiral inductor.

107. The process according to claim 97, further comprising the step of forming at least one passive circuit device for use in radio frequency (RF) communications systems, said passive circuit device having at least one of said plurality of passive circuit elements and electrically connected to said at least one integrated circuit chip.

108. The process according to claim 107, further comprising the step of arranging the interposer element and said at least one integrated circuit to form circuitry for use in RF communications systems.

109. The process according to claim 108, wherein said at least one passive circuit device is for use in a load amplifier.

110. The process according to claim 108, wherein said at least one passive circuit device is for use in a broad band amplifier.

111. The process according to claim 108, wherein said at least one passive circuit device is for use in an oscillator.

112. The process according to claim 111, wherein said oscillator is a voltage controlled oscillator.

113. The process according to claim 108, wherein said at least one integrated circuit chip contains analog circuitry.

114. The process according to claim 108, wherein said at least one integrated circuit chip contains digital circuitry.

115. The process according to claim 114, wherein said integrated circuit chip is a microprocessor.

116. The process according to claim 114, wherein said integrated circuit chip is a memory chip.

117. The process according to claim 108, further comprising the step of forming a bonding layer, said bonding layer located in the area between said at least one integrated circuit chip and said insulating layer.

118. The process according to claim 117, wherein said bonding agent is epoxy.

119. The process according to claim 118, further comprising the step of encapsulating the interposer element and said at least one integrated circuit to form a circuit package, said circuit package having conducting leads on an outer side of said package.

120. The process according to claim 119, further comprising the step of providing conductive leads connecting the interposer element and said at least one integrated circuit to said conductive package leads of said circuit package.

121. The process according to claim 120, further comprising the step of providing an insulating layer to both surfaces of said silicon substrate.

122. The process according to claim 121, further comprising the step of processing said insulating layer to produce at least one active circuit element.

123. The process according to claim 88, said step of processing said insulating layer further comprising the step of providing at least one passive circuit element in each of a plurality of areas of said insulating layer, dividing said silicon substrate into said areas, and bonding at least one integrated circuit chip to each of said areas of said insulating layer to form respective chip carriers.